

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,122,414 B2  
APPLICATION NO. : 10/601037  
DATED : October 17, 2006  
INVENTOR(S) : Hannu Huotari

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

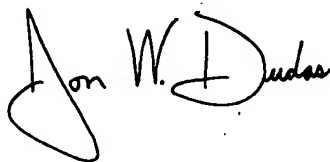
Title Page Illustration Figure(s) Should Be Deleted, And Replaced With The Attached Title Page.

Please replace the drawings of sheets 1-22 with the attached drawings.

In Column 13, line 3, Claim 26, after "HfSi<sub>x</sub>N<sub>y</sub>" please delete "," and insert --;--, therefor.

Signed and Sealed this

First Day of April, 2008

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS  
*Director of the United States Patent and Trademark Office*

(12) **United States Patent**  
**Huotari**

(10) **Patent No.:** **US 7,122,414 B2**  
(45) **Date of Patent:** **Oct. 17, 2006**

(54) **METHOD TO FABRICATE DUAL METAL CMOS DEVICES**

(75) **Inventor:** Hannu Huotari, Espoo (FI)

(73) **Assignee:** ASM International, Inc., Bilthoven (NL)

(\*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** 10/601,037

(22) **Filed:** Jun. 19, 2003

(65) **Prior Publication Data**

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**Related U.S. Application Data**

(60) **Provisional application No.** 60/430,960, filed on Dec. 3, 2002.

(51) **Int. Cl.**  
**H01L 21/8238** (2006.01)

(52) **U.S. Cl.** ..... 438/199; 438/275; 438/592; 257/369; 257/407; 257/412; 257/E21.002

(58) **Field of Classification Search** ..... 257/369, 257/388, 407, 412, 751; 438/199, 275, 592  
See application file for complete search history.

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**Primary Examiner**—Zandra V. Smith

**Assistant Examiner**—Christy L. Novacek

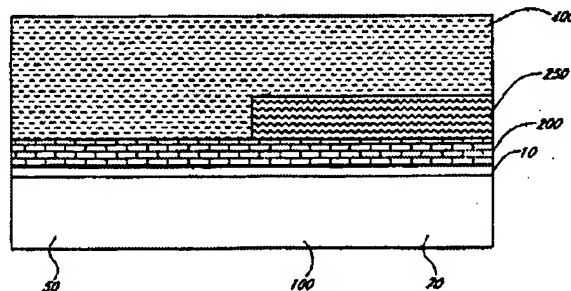
(74) **Attorney, Agent, or Firm**—Knobbe, Martens, Olson & Bear, LLP

(57) **ABSTRACT**

The present invention relates generally to barrier layers in transistor gate stacks in integrated circuits, and to processes for forming such gate stacks.

**28 Claims, 22 Drawing Sheets**

Chemical mechanical polishing (CMP)

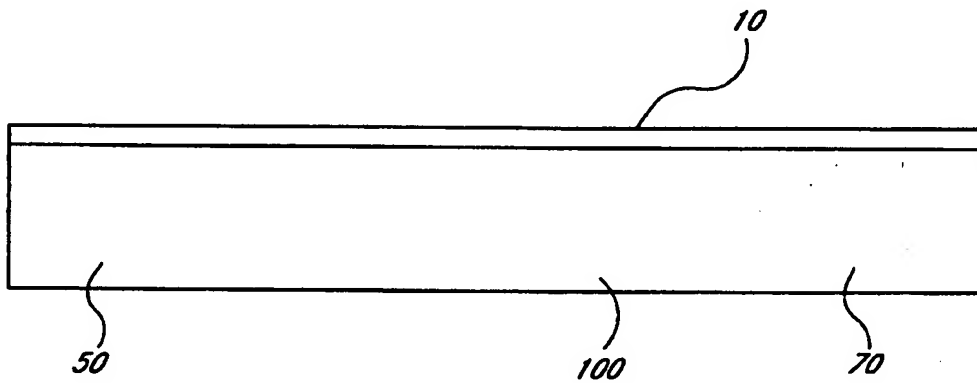


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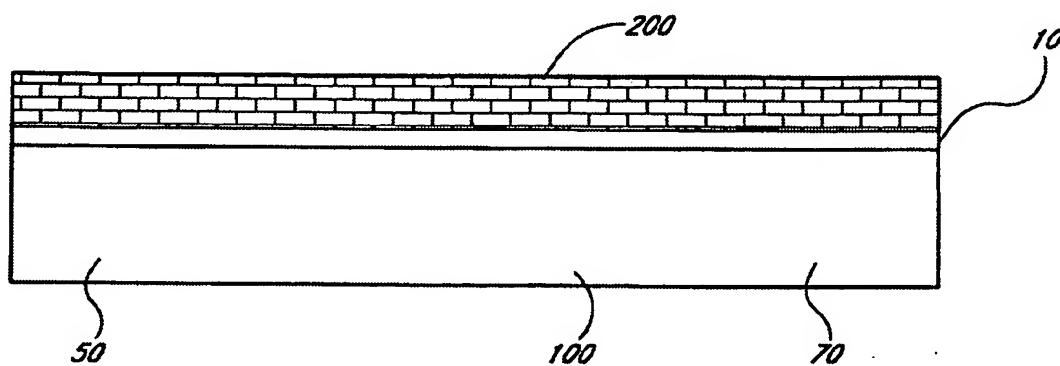
**FIG. 1**

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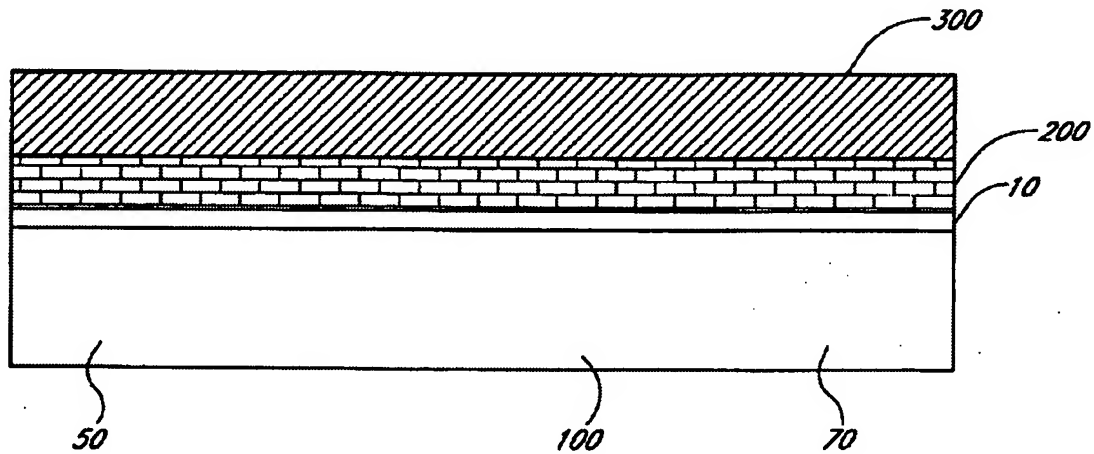
**FIG.2**

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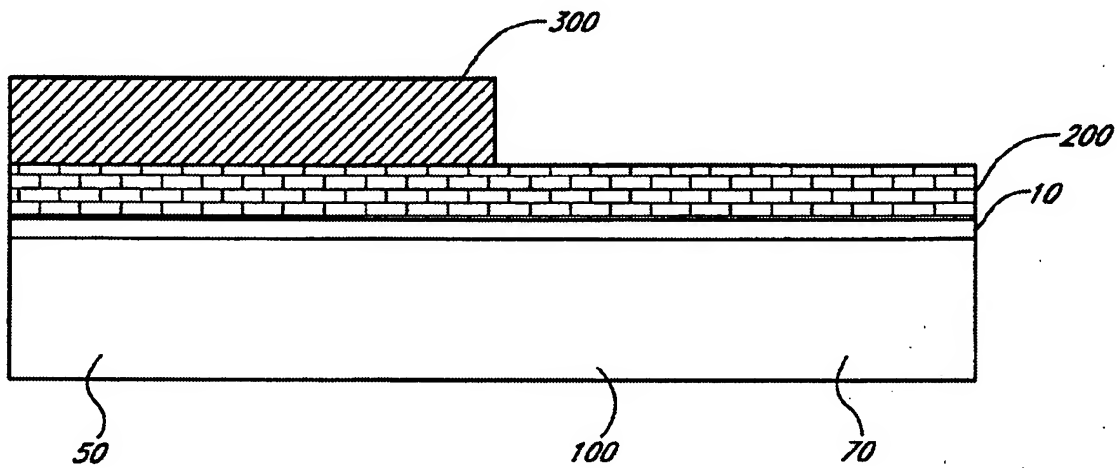
**FIG. 3**

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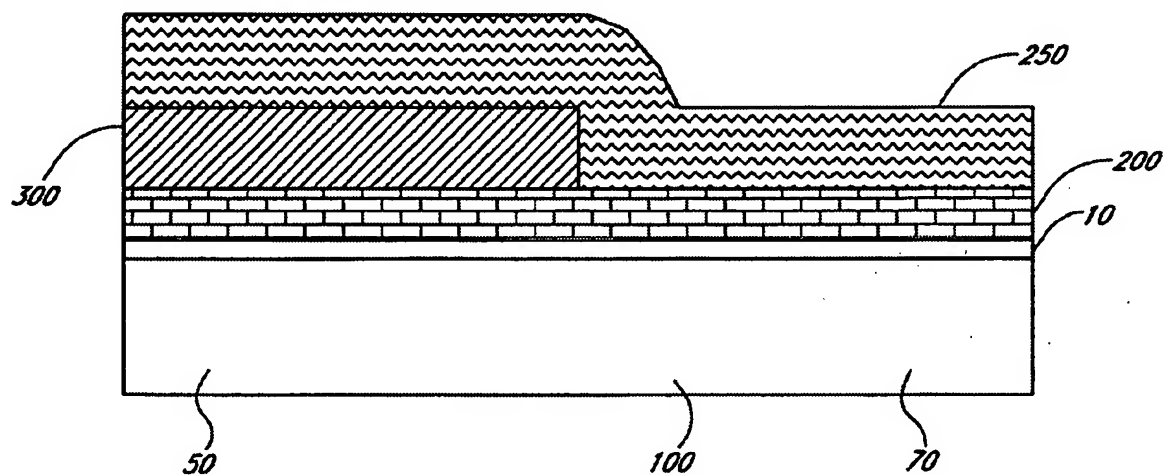
**FIG. 4**

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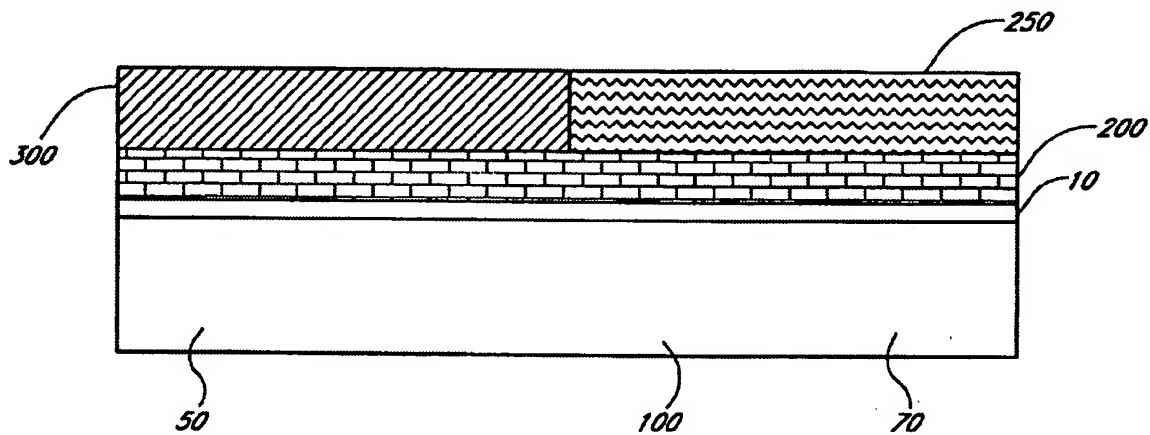
**FIG. 5**

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**FIG. 6**

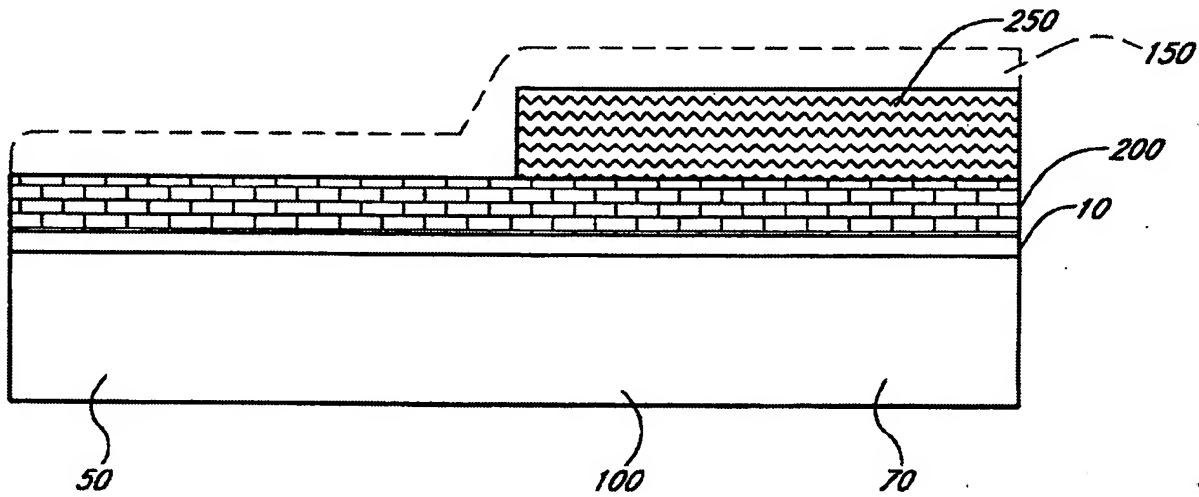


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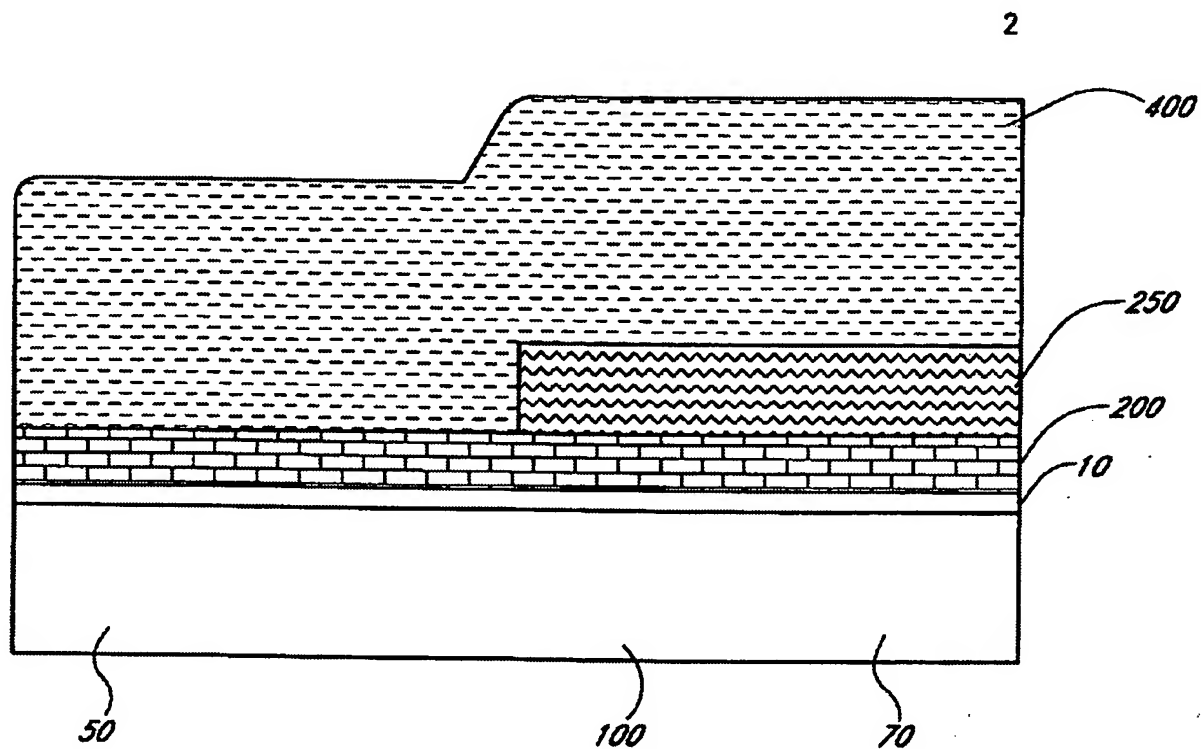
**FIG. 7**

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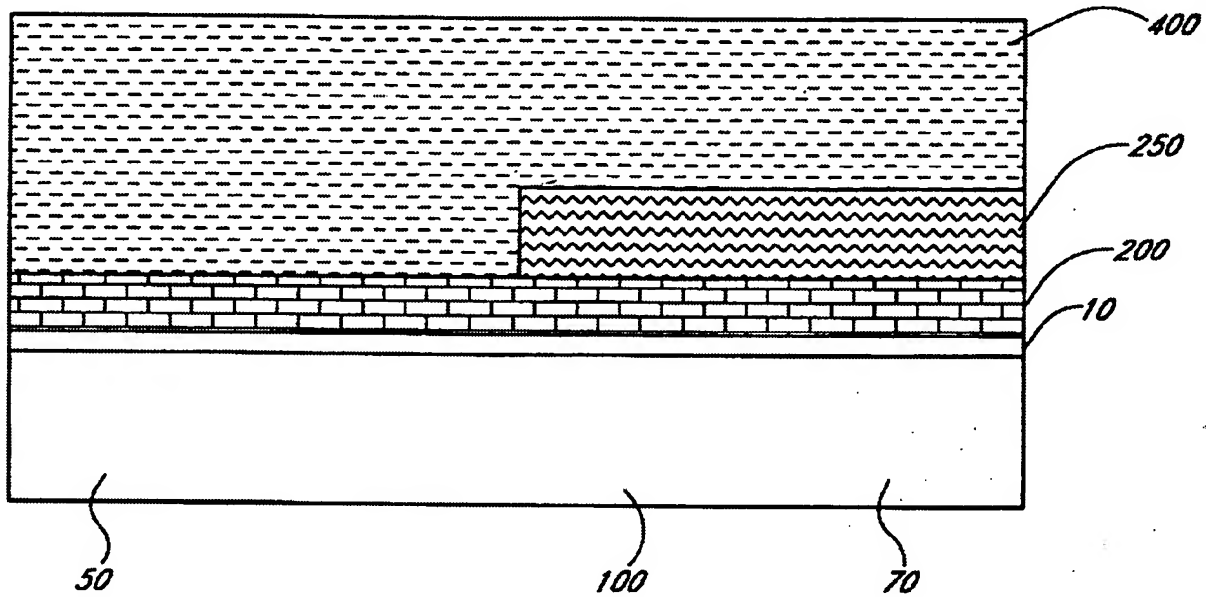
**FIG. 8**

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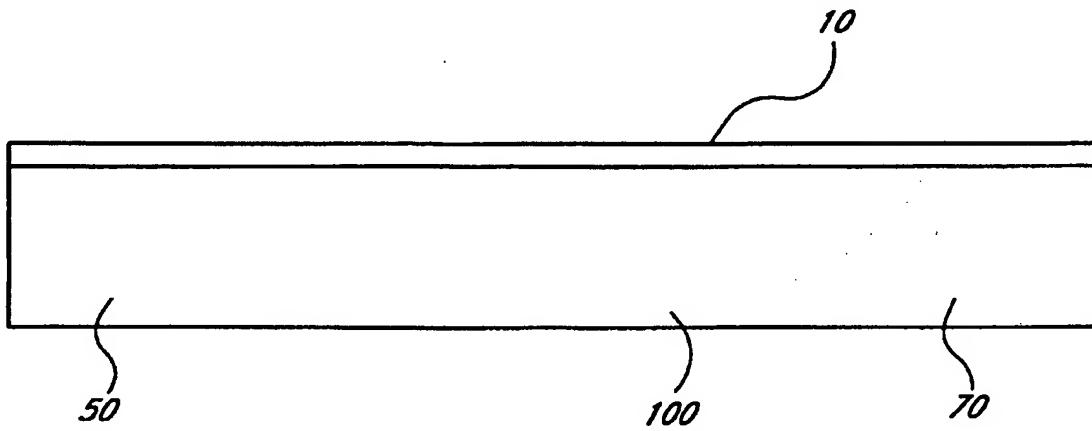
**FIG. 9**

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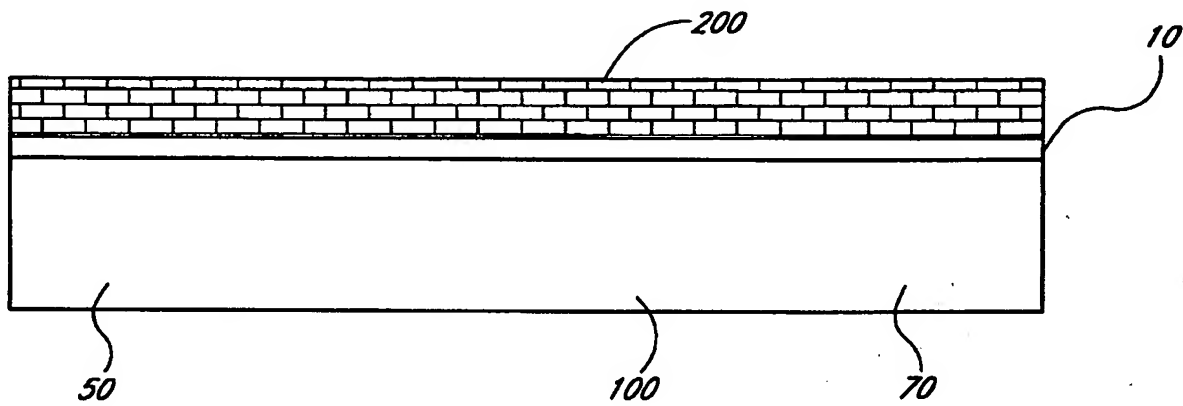
**FIG. 10**

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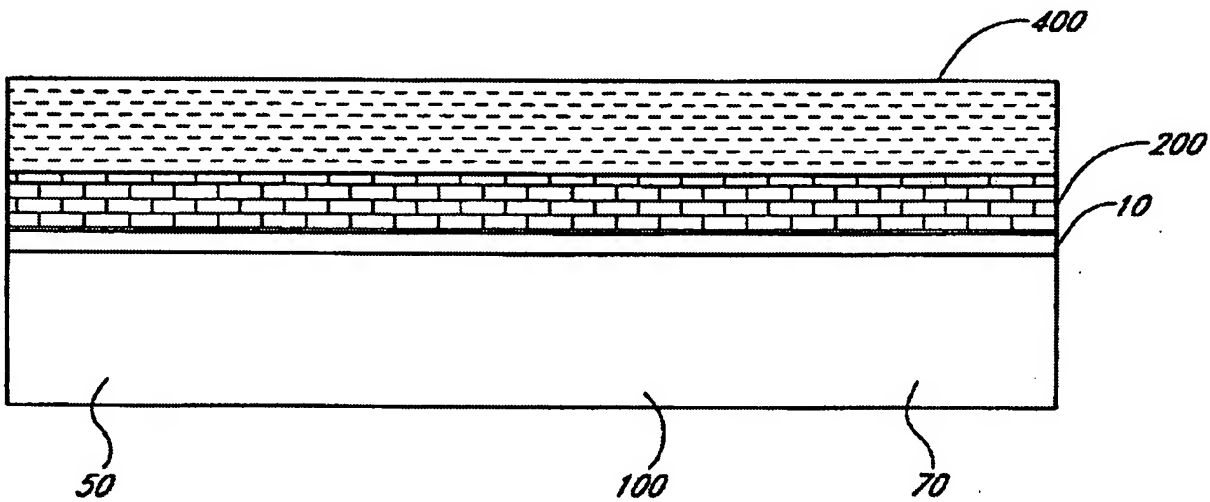
**FIG. 11**

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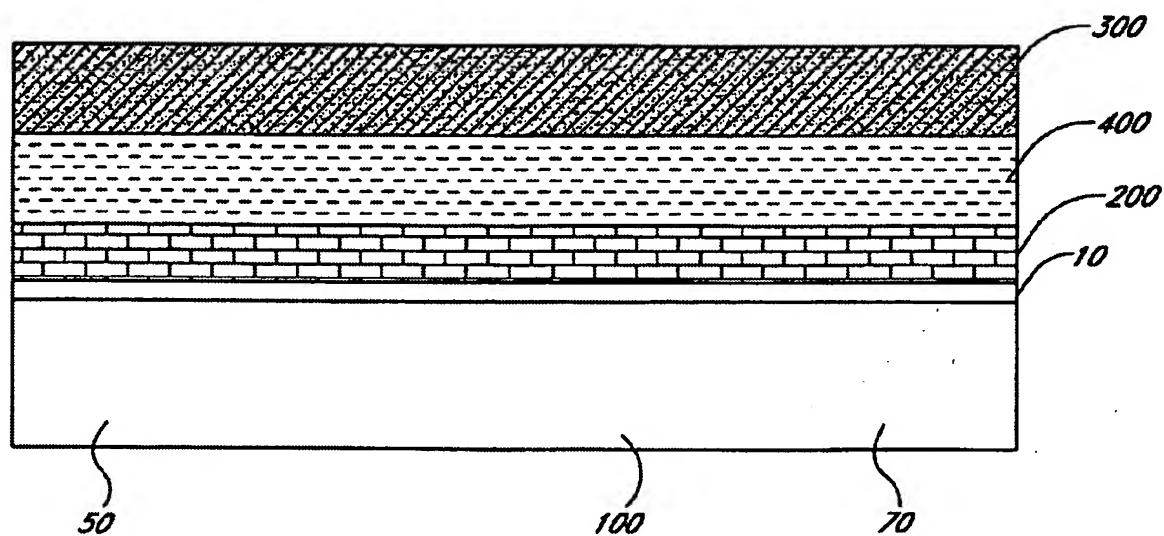
**FIG. 12**

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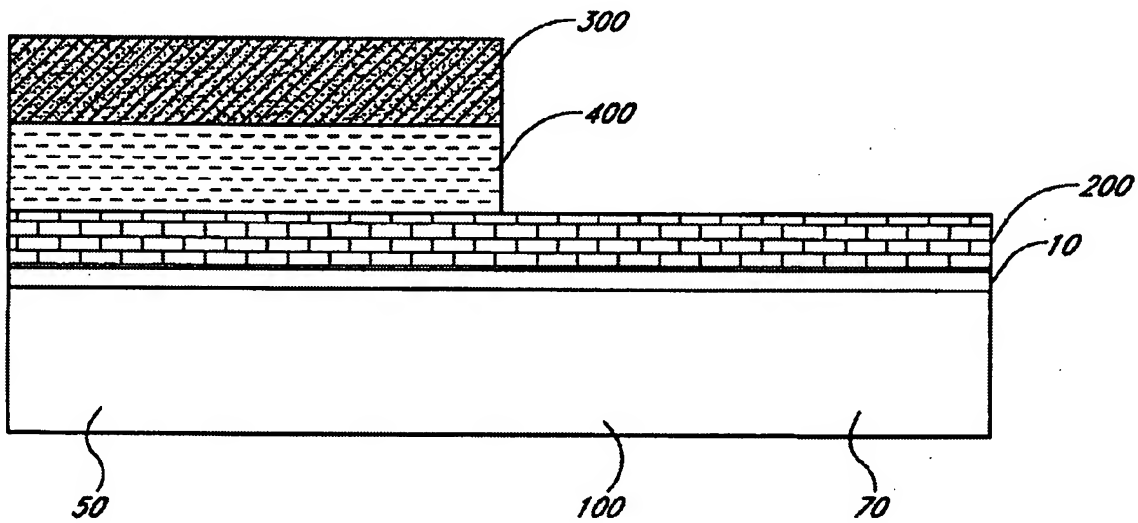
**FIG. 13**

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**FIG. 14**

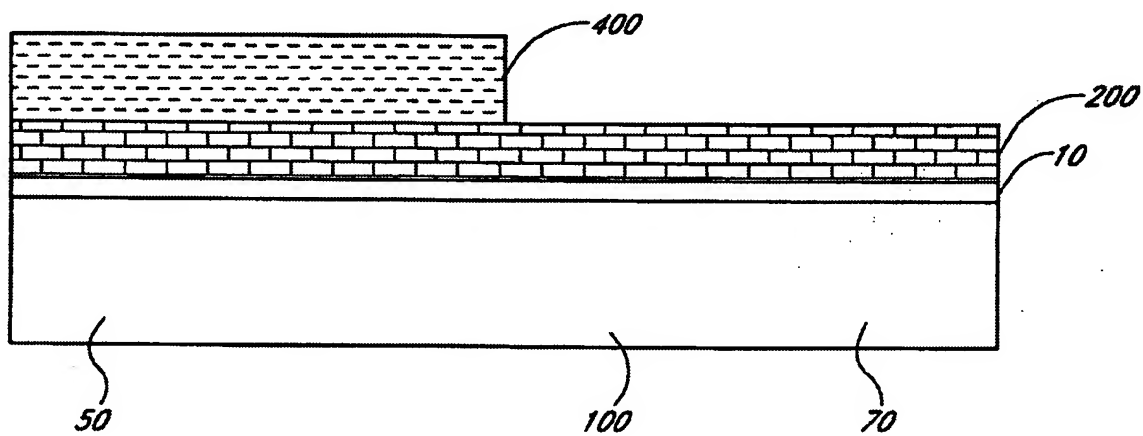


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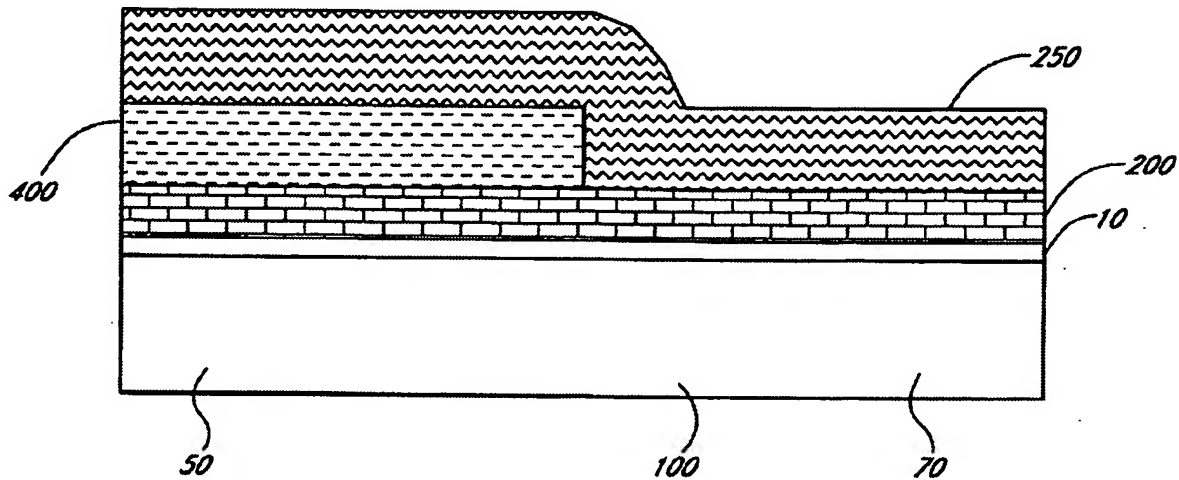
**FIG. 15**

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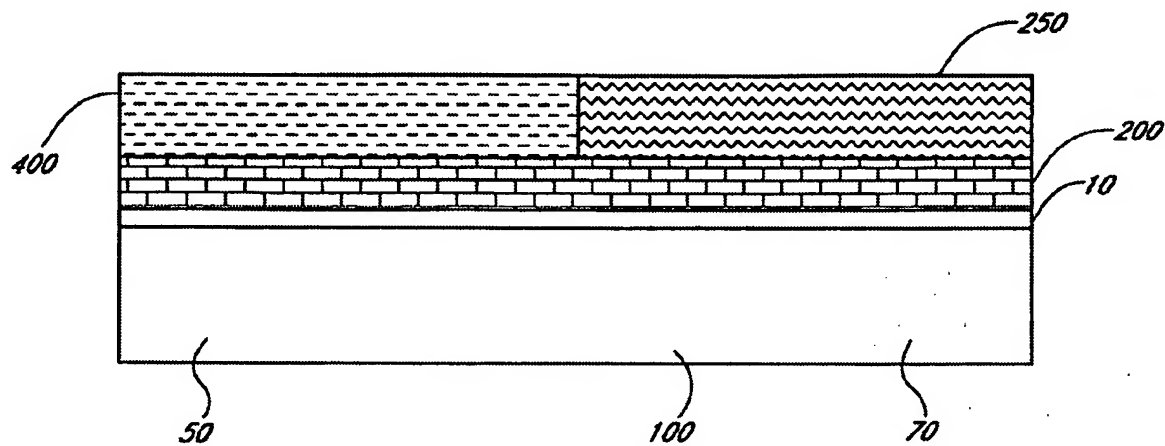
**FIG. 16**

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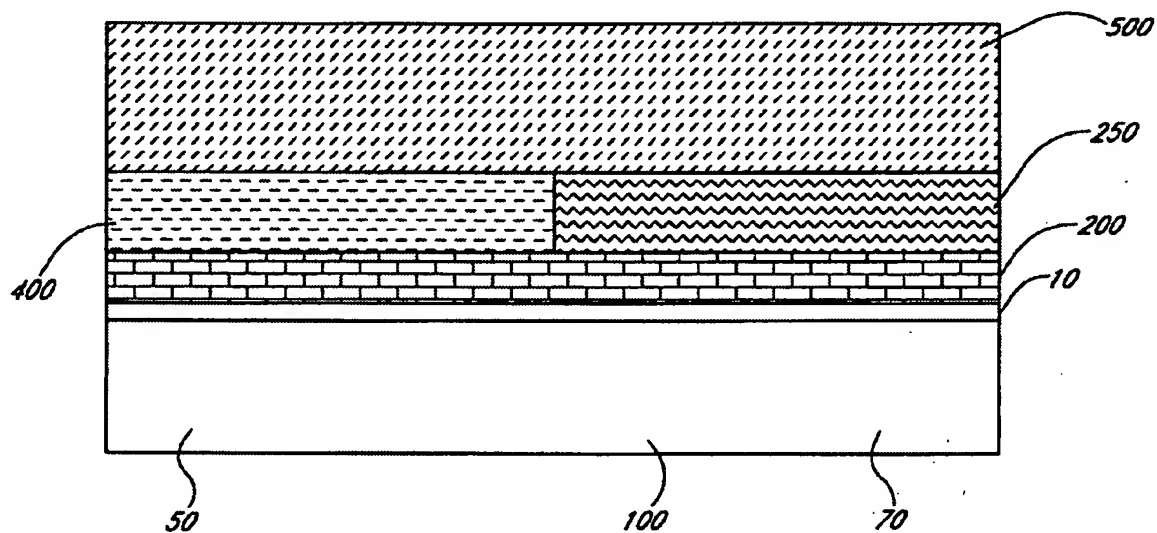
**FIG. 17**

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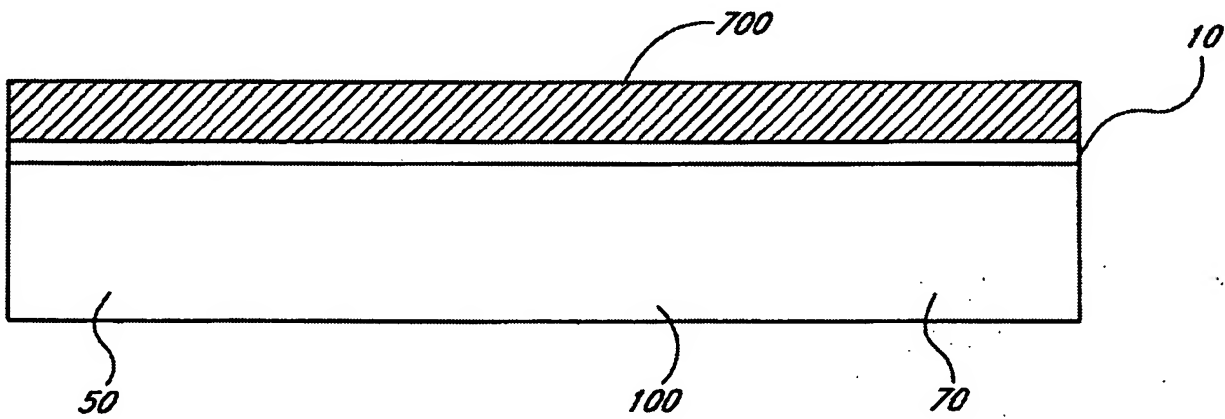
**FIG. 18**

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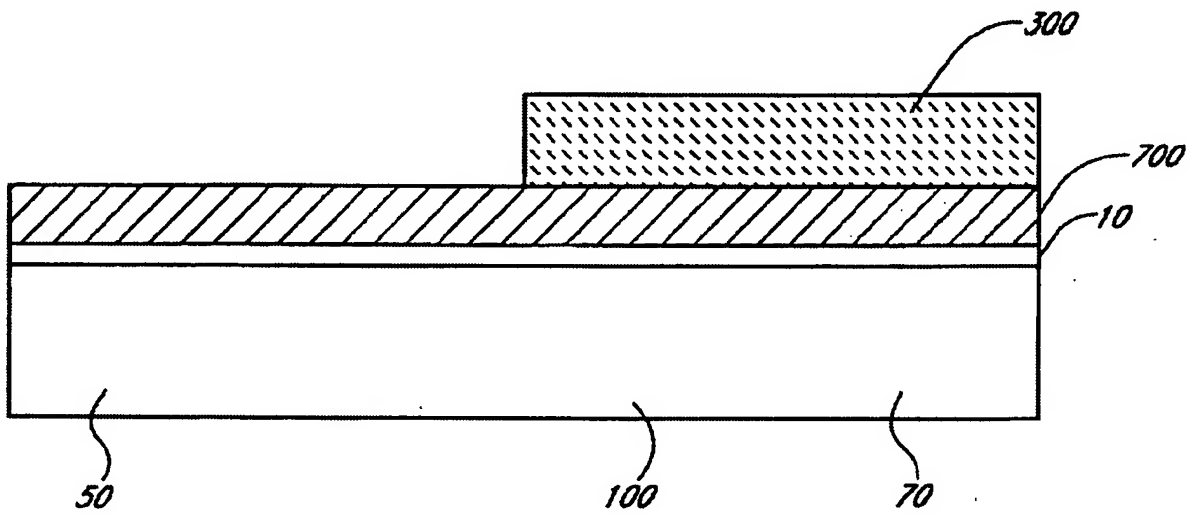
**FIG. 19**

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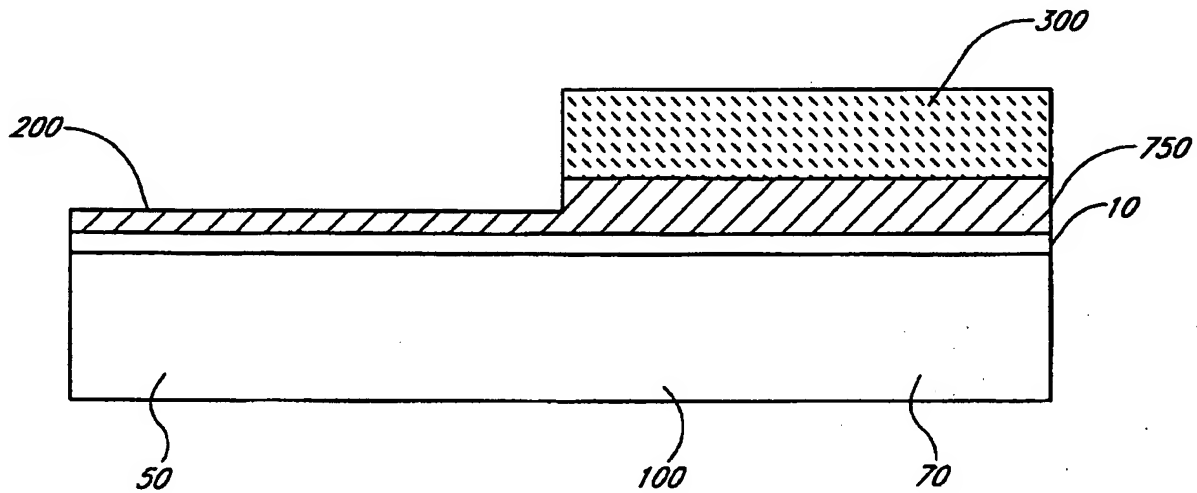
**FIG. 20**

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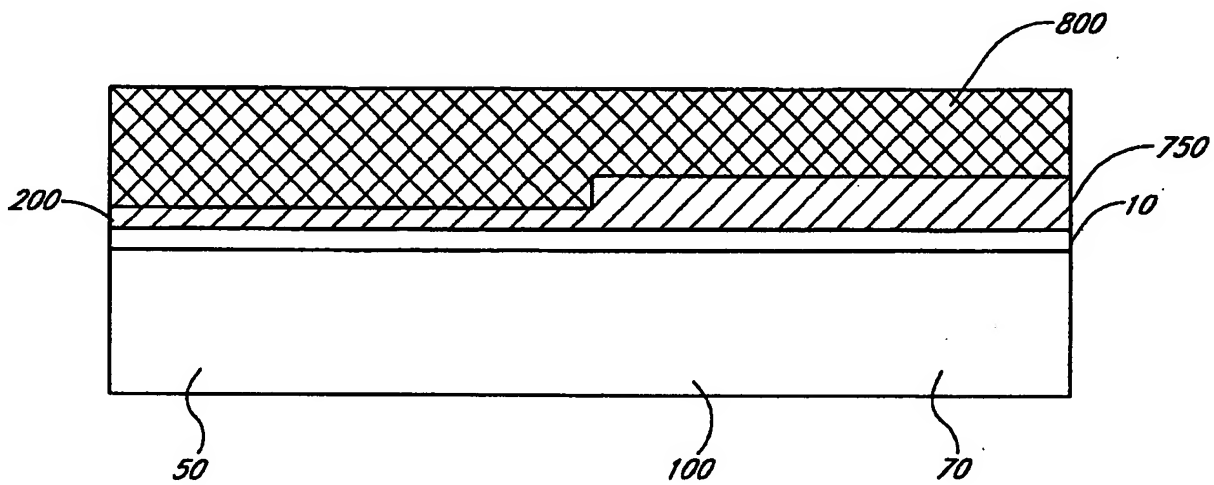
**FIG. 21**

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**FIG.22**